Attorney Docket No. SEL 171

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF APPEALS AND INTERFERENCES

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| In Re Application of: | | ) |
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| | Masaya KADONO et al. | ) |
| | | ) |
| Serial No.: | 09/535,233 | ) |
| | | ) |
| Filed: | March 24, 2000 | ) |
| | | ) |
| For: | A Method Of Manufacturing A Semiconductor Device | ) |
| | | ) |
| Examiner: | William D. Coleman | ) |
| | | ) |
| Art Unit: | 2823 | ) |

## APPEAL BRIEF UNDER 37 C.F.R. 41.37

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## APPEAL BRIEF UNDER 37 C.F.R. §41.37

This Brief is in furtherance of the Notice of Appeal filed in this Application Serial No. 09/535,233 on November 27, 2006.

This appeal is in response to the Final Rejection of August 1, 2006 and the Advisory Action of November 13, 2006 rejecting Claims 11-36.

Claims 11-36 of the present application are clearly patentable over the cited references, as will be shown *infra*, and Appellants respectfully request the Board to so rule and allow the application.

## i. STATEMENT OF REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee: Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan.

## ii. STATEMENT OF RELATED APPEALS AND INTERFERENCES

To the best of Appellants', Appellants' legal representatives' and Assignee's knowledge, there are no appeals or interferences pending which will affect or be affected by the Board's decision in this appeal.

## iii. STATUS OF CLAIMS

Claims 1-42 are pending in this application. Claims 1-10 have been withdrawn. Claims 37-42 have been allowed. Claims 11-36 are rejected. Claims 11-36 are the appealed claims and appear *infra* at p. 20 *et seq.*

## iv. STATUS OF AMENDMENTS

No amendment after final has been filed in this application.

## v. SUMMARY OF CLAIMED SUBJECT MATTER

In accordance with §41.37(c)(v), Appellants are providing the following concise explanation of the claimed subject matter. Appellants are providing examples of where each claim element is shown or discussed in the specification and drawings of the present application. These citations are merely examples, as the application has further disclosure of these elements throughout the application.

The dependent claims are based, either directly or indirectly, on one of the independent claims, and accordingly, all the elements listed for the respective independent claims, and the support for these elements in the specification and drawings, are as mentioned herein. These dependent claims also add additional elements or limitations which are supported in the specification and drawings.

Independent Claim 11 is directed to a method of manufacturing a semiconductor device **(page 12, line 7 et seq.)**, comprising steps of:

forming a semiconductor film **(150)** over a substrate **(101)** having an insulating surface **(page 12, line 10 - page 13, line 3; Fig. 1A)**;

forming a patterned resist mask over said semiconductor film **(page 15, lines 17-21; Fig. 1C)**;

patterning said semiconductor film to form at least one semiconductor island **(104, 105) (page 15, lines 17-21; Fig. 1C)**;

removing the patterned resist mask located over said semiconductor island **(page 15, lines 17-24; Figs. 1C-1D)**;

spinning the substrate after removing the patterned resist mask **(page 16, lines 1-2)**;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution **(page 15, line 22 - page 16, line 12; Figs. 1C-1D)**; and then

forming a gate insulating film **(106)** in contact with the semiconductor film from the surface of which the contaminating impurity has been removed **(page 16, lines 13-16; Fig. 1E)**.

Independent Claim 15 is directed to a method of manufacturing a semiconductor device **(page 12, line 7 et seq.)**, comprising steps of:

forming a semiconductor film **(150)** over a substrate **(101)** having an insulating surface **(page 12, line 10 – page 13, line 3; Fig. 1A)**;

forming a patterned resist mask over said semiconductor film **(page 15, lines 17-21; Fig. 1C)**;

patterning said semiconductor film to form at least one semiconductor island **(104, 105) (page 15, lines 17-21; Fig. 1C)**;

removing the patterned resist mask located over said semiconductor island **(page 15, lines 17-24; Figs. 1C-1D)**;

spinning the substrate after removing the patterned resist mask **(page 16, lines 1-2)**;

applying an etching solution to a surface of said semiconductor island and scattering the

etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution **(page 15, line 22- page 16, line 12; Figs. 1C-1D)**;

forming a gate insulating film **(106)** over said semiconductor island after the contaminating impurities are removed from the surface of the semiconductor island **(page 16, lines 13-16; Fig. 1E)**;

spinning the substrate having the gate insulating film **(page 18, lines 1-8; Fig. 2B)**;

applying an etching solution to a surface of said gate insulating film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the gate insulating film by the step of applying the etching solution **(page 18, lines 1-8; Fig. 2B)**; and then

forming a gate electrode **(112)** over said gate insulating film after the contaminating impurities are removed from the surface of the gate insulating film **(page 18, line 9 – page 19, line 9: Fig. 2C)**.

Independent Claim 19 is directed to a method of manufacturing a semiconductor device **(page 12, line 7 et seq.)**, comprising steps of:

forming a semiconductor film **(150)** over a substrate **(101)** having an insulating surface **(page 12, line 10 – page 13, line 3; Fig. 1A)**;

crystallizing said semiconductor film **(page 14, lines 10-16)**;

forming a patterned resist mask over said crystallized semiconductor film **(page 15, lines 17-21; Fig. 1C)**;

patterning the crystallized semiconductor film to form at least one semiconductor island

**(104, 105)** over said substrate **(page 15, lines 17-21; Fig. 1C)**;

removing the patterned resist mask located over said semiconductor island **(page 15, lines 17-24; Figs. 1C-1D)**;

spinning the substrate after removing the patterned resist mask **(page 16, lines 1-2)**;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island **(page 15, line 22 - page 16, line 12; Figs. 1C-1D)**; and then

forming a gate insulating film **(106)** over said semiconductor island after the contaminating impurities are removed from the surfaces by the step of applying the etching solution **(page 16, lines 13-16; Fig. 1E)**; and

forming a gate electrode **(112)** over said gate insulating film **(page 18, line 9 – page 19, line 9; Fig. 2C)**.

Independent claim 23 is directed to a method of manufacturing a semiconductor device **(page 25, line 8 et seq.)**, comprising steps of:

forming a gate wiring **(802)** over a substrate **(801)** having an insulating surface **(page 25, lines 11-22; Fig. 8A)**;

spinning the substrate **(page 26, lines 3-17; Fig. 8B)**;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution **(page 26, lines 3-17; Fig. 8B)**; and then

forming a gate insulating film **(803)** and a semiconductor film **(804)** over said gate wiring after the contaminating impurities are removed from the surfaces **(page 26, lines 18-21)**.

Independent Claim 27 is directed to a method of manufacturing a semiconductor device **(page 25, line 8 et seq.)**, comprising steps of:

forming a gate wiring **(802)** over a substrate **(801)** having an insulating surface **(page 25, lines 11-22; Fig. 8A)**;

spinning the substrate **(page 26, lines 3-17; Fig. 8B)**;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution **(page 26, lines 3-17; Fig. 8B)**; and then

forming a gate insulating film **(803)** and a semiconductor film **(804)** over said gate wiring, continuously after the contaminating impurities are removed from the surfaces **(page 26, lines 18-21)**.

Claims 12, 17, 21, 25 and 29 are dependent on Claims 11, 15, 19, 23 and 27, respectively, and recite that the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements **(page 2, lines 9-13; page 9, lines 8-10)**.

Claims 13, 18, 22, 26 and 30 are dependent of Claims 11, 15, 19, 23, and 27, respectively, and recite that the contaminating impurity element is at least one element selected from the group consisting

of Na, K, Mg, Ca, and Ba **(page 2, lines 9-13; page 9, lines 8-12)**.

Claims 14 and 32-35 are dependent on Claims 11, 15, 19, 23 and 27, respectively, and recite that the contaminating impurity is removed by an acidic solution containing fluorine **(page 6, lines 16-18; page 15, line 24 – page 16, line 12; page 26, lines 3-17)**.

Claims 16, 20, 24, 28 and 31 are dependent on Claims 11, 15, 19, 23 and 27, respectively, and recite that said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500) **(page 6, line 22 - page 7, line 3; page 15, line 24 – page 16, line 12; page 26, lines 3-17)**.

Claim 36 is dependent on claim 19 and recites that the step of crystallization is performed by irradiating the semiconductor film with a laser light **(page 13, lines 6-7; page 14, line 17 - page 15, line 7)**.

## vi. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following are the grounds for rejection presented for review:

A. Claims 11-18, 23-32 and 34-35 are rejected under 35 USC §102(b) as being anticipated by Konuma (US 6,127,279)

B. Claims 19-22 and 36 are rejected under 35 USC §102(b) as being anticipated by Chiyou et al. (JP 11-016866).

## vii. ARGUMENT

### A. BACKGROUND

The present application is directed to a method for manufacturing a semiconductor device, such as a thin film transistor (TFT).

When evaluating and manufacturing a TFT, one of the most important characteristics is reliability. With reliability, one of the biggest concerns is that an alkaline metal (periodic table group 1 element), a mobile ion, particularly sodium (Na), becomes mixed in. This problem is presented as a phenomenon in which Na is electrified to have a positive electric charge and Vth changes by Na moving as an ion throughout the film, preventing the practical use of the TFT. Examples of this type of impurity (hereafter, impurities such as Na which cause decrease in the reliability of a TFT are referred to as contaminating impurities) include: alkaline metals (periodic table group 1 elements) and alkaline earth metals (group 2 elements), such as sodium (Na), potassium (K), magnesium (Mg), calcium (Ca), and barium (Ba). The reduction of these contaminating impurities is crucial for the manufacture of reliable TFTs.

Contaminating impurities can get mixed into TFTs from a variety of impurity sources, such as gases in the atmosphere or high pressure gas cylinders, glass substrates, and manufacturing apparatuses such as a sputtering device. One particular serious problem is contamination from a glass substrate. Even by using a glass substrate with a Na composition of 0.1% or lower, this reliability problem has not been solved. One solution to this problem is forming a blocking film, such as a silicon nitride film, on the substrate, to prevent contaminating impurities contained in the glass substrate from diffusing and lowering reliability.

However, contaminating impurities still exist. As a result of analyzing the contaminating impurity concentration in a TFT, it was determined that the contaminating impurity concentration of the interface between films structuring the TFT is between 5 x $10^{16}$ atoms/$cm^3$ and 5 x $10^{19}$ atoms/$cm^3$, which is higher than the contaminating impurity concentration within the films (generally 1 x $10^{16}$ atoms/$cm^3$ or less), and indicates that this is a major cause of the reduction in TFT reliability. Hence, a contaminating impurity that exists in the interface between a semiconductor film and an insulating film in contact with the semiconductor film (the insulating film can be a gate insulating film, a blocking film, or a interlayer insulating film), or in the interface between the gate insulating film and a film contacting the gate insulating film (such as the semiconductor film, a gate wiring or a gate electrode, or an interlayer insulating film), is a major cause of loss of TFT reliability. See e.g. pages 1-4 of the specification of the present application.

Accordingly, it was an objective of the present invention to lower the concentration of a contaminating impurity, not only within a film for forming a TFT but also in a film interface, to a concentration level which does not have a negative influence on the reliability of a TFT.

In order to realize this objective, the method of the present invention is characterized in that after forming a first film, a contaminating impurity is removed from the surface of the first film before forming a second film on the first film, and the second film is formed on the surface of the first film from which the contaminating impurity has been removed as quickly as possible. By forming the next film, without exposing the film surface to the atmosphere or to contaminating impurities, impurity contamination in the film interfaces can be prevented. As a result, one cause of the development of dispersion in TFT characteristics and decreases in reliability can be eliminated. The present invention achieves this through the steps recited in the claims of the present application.

As explained below, the methods of the cited references differ from the steps of the claimed methods and cannot achieve this objective.

Appellants will now address the pending rejections of the claims from the Final Rejection of August 1, 2006 (the Advisory Action of November 13, 2006 including no further comments or rejections).

## B. THE REJECTIONS OF THE CLAIMS SHOULD BE REVERSED

### 1. For Anticipation, Each And Every Claim Element Must Be In The Reference

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Absence of a claim element from a prior art reference negates anticipation. *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 224 USPQ 409, 411 (Fed. Cir. 1984); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81, 84 (Fed. Cir. 1986), cert. denied, 479 US 1034 (1987).

In this case, both of the Examiner's rejections are §102 anticipation rejections. As shown below, the cited reference in each rejection does not show each and every element set forth in the claims. Accordingly, the anticipation rejections should be reversed or withdrawn.

### 2. Konuma Does Not Show Every Claim Element

The Examiner rejects Claims 11-18, 23-32 and 34-35 under 35 USC §102(b) as being anticipated by Konuma (US 6,127,279). The Examiner's rejection, however, is erroneous as each and every claim element is not found in Konuma. The rejection is also improper as the Examiner has

not shown each and every claim element.

a. Claims 11-18, 31 and 32

For example, independent Claim 11 is directed to a method of manufacturing a semiconductor device including the steps of:

> "forming a patterned resist mask over said semiconductor film;
>
> patterning said semiconductor film to form at least one semiconductor island;
>
> removing the patterned resist mask located over said semiconductor island;
>
> spinning the substrate after removing the patterned resist mask."

The claim recites as the final step "and then forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed" (emphasis added). Independent Claim 15 includes similar claimed steps.

All of these steps are not disclosed in Konuma nor are the steps in Konuma in the same order as in the claimed method.

At page 8 of the Final Rejection, the Examiner states that with regard to the step of "forming a patterned resist mask over said semiconductor film", that element is "not shown."[1] With regard to the step of "patterning said semiconductor film to form at least one semiconductor island," the Examiner provides no explanation or statement in this section as to where this feature is shown. The step of "removing the patterned resist mask located over said semiconductor island" is not listed or discussed at all in this section. The Examiner also provides no showing in this section of where the

1 Throughout the Final Rejection, the Examiner continually states that "Konuma would suggest" or "this would suggest." Such an analysis seems to indicate an obviousness rejection and not an anticipation rejection

claimed feature of "forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed" is shown in Konuma.

On pages 5-6 of the Final Rejection, the Examiner appears to be arguing that these steps are suggested in Konuma. In particular, the Examiner states that with reference to "FIG. F [sic 1F] and FIG 8B" that:

> "First and foremost we know that the figure to the left [Fig. 1F] discloses a thin film transistor (TFT) as a final product of a solution applying method as claimed. The semiconductor device contains a substrate **101** (Corning #7059, which has alkali metals which are undesirable as discussed above), next a base film **102** comprising a silicon oxide film is formed above the substrate, next an island like film **103** is formed by patterning the silicon film (see column 7, lines 4-6), next an aluminum film with a thickness of 6000 Å is formed on the silicon film and a photo resist is applied to the upper surface of the aluminum film by spin coating, it is then subsintered at 90°C, exposed to light, developed, main-sintered, and patterned, thereby forming a hardened photoresist **105**. It is well known to a coat substrate, semi-cure or semi-dry the photoresist before exposing it to light to form a patterned resist film. Next, the substrate is then introduced into a chamber of a spin etching apparatus so that the spin etching forms the gate electrode (because Applicants are aware of the disclosure of this pertinent information, it can be found in column 7, lines 8-14). The Examiner believes that Konuma would suggest forming the silicon island by spin etching because Konuma teaches that is possible to uniformly apply a solution to a substrate on which a resist is formed by ultraviolet light irradiation or ozone water contact to the surface of the resist because, to decrease a contact angel of the solution, in solution applying method in which the moving speed of etching solution over the surface of the substrate is high (column 16, lines 46-52). This would suggest that spin etching can be used not only for the gate electrode but for any film on the substrate as described by Konuma."

Initially, Applicants note that the Examiner's recital of the disclosure in Konuma is faulty. For example, in Konuma, *prior* to the aluminum film being formed and the photoresist (105) applied, a gate insulating film (104) is formed. See col. 7, lines 5-9 and Fig. 1A (which is different then the method of Claim 11, as discussed *infra*). Thereafter, the substrate (101), with the gate insulating film (104) thereover and the resist (105) over gate insulating film (104), "is then introduced" into the chamber for spin etching. See col. 7, lines 5-16. This is clearly different than the claimed invention

wherein the spinning of the substrate occurs after removing the patterned resist mask (and prior to forming the gate insulating film). Therefore, Konuma does not disclose at least the steps of "removing the patterned resist mask located over said semiconductor island" and "spinning the substrate after removing the patterned resist mask."

In addition, Konuma also does not disclose the step of Claims 11 and 15 of applying etching solution to a surface of the semiconductor island. The Examiner cites col. 7, lines 65-68 for allegedly showing this feature. This sentence merely states that before etching the substrate may be cleaned. Nothing is mentioned in Konuma about cleaning the semiconductor island, especially not prior to forming the gate insulating film over the cleaned semiconductor island. Therefore, Konuma does not disclose this step of independent Claims 11 and 15.

Further, as shown above, Konuma does not disclose these steps in the order recited in Claims 11 and 15.

Furthermore, independent Claim 11 recites as the last step "and then forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed." Claim 15 is similar. In contrast, Konuma discloses forming a semiconductor film, then forming a gate insulating film (104) over the semiconductor film (103) (col. 7, lines 5-8; Fig. 1A), and "after this" forming an aluminum film and applying a photoresist to the aluminum film and then forming a hardened photoresist (105). Col. 7, lines 9-15. The substrate (with the above layers) "is then introduced into a chamber" for spin etching. Col. 7, lines 16-17. Hence, in Konuma, the gate insulating film is formed *prior* to etching and is not formed on a surface from which the contaminating impurity has been removed, as in Claims 11 and 15. As explained

above, in the Background section at p. 8-10, this claimed step is highly advantageous for increasing the reliability of the resulting TFT.

Further, Konuma does not disclose forming the gate insulating film after removing the patterned resist mask and as a result, does not disclose the steps of independent Claims 11 and 15 in the order recited in the claims.

Accordingly, many of the claim elements of the method of independent Claims 11 and 15, and those claims dependent thereon, are not disclosed in Konuma, and Claims 11-18, 31 and 32 cannot be anticipated by Konuma.

b. Claims 23-30, 34, 35

With regard to independent Claims 23 and 27, the Examiner provides no explanation or showing as to where the claimed features are shown in Konuma. Further, the claim elements of these claims are not disclosed in Konuma. For example, Claims 23 and 27 recite in general the steps of forming a gate wiring over a substrate, spinning the substrate, applying an etching solution to surfaces of said substrate and said gate wiring to remove impurities, and then forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces.

As explained above, in Konuma, a semiconductor film 103 is formed, then a gate insulating film 104 is formed, then an aluminum film (which becomes gate electrode 106) is formed, then the hardened photoresist 105 is formed, and then the entire structure of substrate, semiconductor film, gate insulating film and hardened photoresist are introduced into the spin etching apparatus chamber. See Col. 7, lines 4-17 in Konuma. This is clearly different than the method of Claims 23 and 27

described above wherein a gate wiring is formed, then the substrate is spinned and cleaned, and then a gate insulating film is formed over the cleaned surface. Hence, Konuma does not disclose many of the claim elements of independent Claims 23 and 27.

Further, the Examiner merely contends that "since Konuma teaches the fabrication of various semiconductor devices, the wiring layer is inherent." However, not only does Konuma not disclose the claimed method as explained above, but the Examiner's allegation of this one claim feature as being "inherent" is an insufficient showing for an anticipation rejection.

Therefore, since Konuma does not disclose the claimed feature of forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces, as recited in Claims 23 and 27 (and other claimed features as discussed above), and there has been no showing as to how Konuma discloses these features, independent Claims 23 and 27 and those claims dependent thereon cannot be anticipated by Konuma.

c. Conclusion Regarding Rejection Over Konuma

As explained above, many of the claim elements of independent Claims 11, 15, 23 and 27 are not disclosed in Konuma. Therefore, Claims 11-18, 23-32, 34 and 35 cannot be anticipated by Konuma. Accordingly, this the rejection of Claims 11-18, 23-32, 34 and 35 as being anticipated by Konuma should be reversed or withdrawn.

3. Chiyou Does Not Show Every Claim Element

The Examiner also rejects Claims 19-22 and 36 under 35 USC §102(b) as being anticipated by Chiyou et al. (JP 11-016866). The Examiner's rejection, however, is erroneous as each and every

claim element is not found in Chiyou. The rejection is also improper as the Examiner has not shown each and every claim element.

As explained *supra*, in order for there to be anticipation, each and every claim element must be found in the reference. Chiyou does not disclose each and every claimed element.

For example, the Examiner contends that Chiyou discloses the claimed features of "crystallizing said semiconductor film" at [0052] and "spinning the substrate [0051] after removing the patterned resist mask." Appellants respectfully disagree. Chiyou teaches a spin desiccation for desiccate (drying) a substrate after removal of the natural oxidation film 4. See [0050] - [0053] in Chiyou. Hence, Chiyou does not disclose or suggest the claimed features of "spinning the substrate after removing the patterned resist mask;" and "applying an etching solution to a surface of said semiconductor island and scattering the etching solution *during said spinning*" (emphasis added), as recited in independent Claim 19.

Further, Claim 19 clearly recites an order for the claimed steps:

[a] crystallizing said semiconductor film;

[b] forming a patterned resist mask over said *crystallized semiconductor film* [hence, the semiconductor film must be crystallized];

[c] patterning the *crystallized semiconductor film* to form at least one semiconductor island *over* said substrate;

[d] removing the patterned resist mask located over *said semiconductor island*; [hence, the semiconductor island must be formed]

[e] spinning the substrate [over which the semiconductor island is formed in [c] above] *after* removing the patterned resist mask; [hence, the patterned mask must be formed before it is removed]

(bracketed matter and emphasis added for illustration purposes).

Accordingly, a feature of the claimed method is spinning the substrate over which the crystallized semiconductor island has been formed (i.e. the semiconductor island has been crystallized before spinning).

In contrast, Chiyou's process (i.e. the spin desiccation) in [0051] is *pretreatment* for the laser crystallization in [0052]. Hence, Chiyou does not disclose or suggest spinning the substrate after crystallization, as in the claimed method, but instead the spinning is *prior* to crystallization.

Therefore, Chiyou cannot disclose each of the claim elements and the method of independent Claim 19.

The Examiner also contends that Chiyou discloses "forming a semiconductor island over said substrate by patterning the crystallized semiconductor film" in Drawing 3 of Chiyou. However, Drawing 3 does not teach that the silicon (of a "Surface of Silicon" in Drawings 3A and 3B) is patterned into a semiconductor island in Drawings 3A and 3B or paragraphs [0008] and [0009]. In order to make this clear, Appellants previously prepared and filed a translation of Drawings 3A and 3B (with the Response of November 1, 2006 and entered by the Examiner in the Advisory Action of November 13, 2006). This translation clearly shows evidence of a water drop and a silicon oxide (water mark), and confirms that neither Drawings 3A nor 3B show a semiconductor island. Further, neither drawing shows that silicon is patterned into a semiconductor island.

In addition, with regard to Claim 19, the Examiner appears to be making the following assertions regarding the following claimed features of Claim 19:

"forming a patterned resist mask over said crystallized semiconductor film" is *well known*;

"patterning the crystallized semiconductor film to form at least one semiconductor island

over said substrate" is *inherent*;

"removing the patterned resist mask located over said semiconductor island" is a *necessary requirement* to make functional devices; and

that forming a gate insulating film and a gate electrode are *well known* to be incorporated in the devices taught by Chiyou.

Applicants have challenged the Examiner on these assertions as not being proper, but the Examiner has not provided any explanation or support for his contentions.

Further, an allegation that an element is "well known" or a "necessary requirement" is not a sufficient showing of the claim elements to support an anticipation rejection. Therefore, this §102(b) rejection is improper.

Therefore, for at least the reasons explained above, many of the claim elements of independent Claim 19 are not disclosed in Chiyou. Accordingly, Claim 19 and those claims dependent thereon cannot be anticipated by Chiyou, and this rejection should be reversed or withdrawn.

## C. CONCLUSION

For at least the reasons stated above, Appellants earnestly and respectfully submit that the cited references do not disclose each and every claim element in the rejected claims. Further, the Examiner has failed to show each and every claim element.

Therefore, the rejection of the claims should be reversed, and the appealed claims allowed.

Accordingly, Appellants request that this Appeal be sustained in all respects, and that all rejections in the Final Rejection and Advisory Action be reversed.

Respectfully submitted,

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## viii. CLAIMS APPENDIX

In accordance with 37 CFR 41.37(c)(1)(viii), the text of the claims on appeal is as follows:

11. A method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface;

forming a patterned resist mask over said semiconductor film;

patterning said semiconductor film to form at least one semiconductor island;

removing the patterned resist mask located over said semiconductor island;

spinning the substrate after removing the patterned resist mask;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution; and then

forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed.

12. A method according to claim 11, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements.

13. A method according to claim 11, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

14. A method according to claim 11, wherein the contaminating impurity is removed by an acidic solution containing fluorine.

15. A method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface;

forming a patterned resist mask over said semiconductor film;

patterning said semiconductor film to form at least one semiconductor island;

removing the patterned resist mask located over said semiconductor island;

spinning the substrate after removing the patterned resist mask;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island by the step of applying the etching solution;

forming a gate insulating film over said semiconductor island after the contaminating impurities are removed from the surface of the semiconductor island;

spinning the substrate having the gate insulating film;

applying an etching solution to a surface of said gate insulating film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the gate insulating film by the step of applying the etching solution; and then

forming a gate electrode over said gate insulating film after the contaminating impurities are removed from the surface of the gate insulating film.

16. A method according to claim 15, wherein said etching solution is selected from the group

consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500).

17. A method according to claim 15, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements.

18. A method according to claim 15, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

19. A method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate having an insulating surface;

crystallizing said semiconductor film;

forming a patterned resist mask over said crystallized semiconductor film;

patterning the crystallized semiconductor film to form at least one semiconductor island over said substrate;

removing the patterned resist mask located over said semiconductor island;

spinning the substrate after removing the patterned resist mask;

applying an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the semiconductor island; and then

forming a gate insulating film over said semiconductor island after the contaminating

impurities are removed from the surfaces by the step of applying the etching solution; and

forming a gate electrode over said gate insulating film.

20. A method according to claim 19, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500).

21. A method according to claim 19, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements.

22. A method according to claim 19, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

23. A method of manufacturing a semiconductor device, comprising steps of:

forming a gate wiring over a substrate having an insulating surface;

spinning the substrate;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution; and then

forming a gate insulating film and a semiconductor film over said gate wiring after the contaminating impurities are removed from the surfaces.

24. A method according to claim 23, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500).

25. A method according to claim 23, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements.

26. A method according to claim 23, wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

27. A method of manufacturing a semiconductor device, comprising steps of:

forming a gate wiring over a substrate having an insulating surface;

spinning the substrate;

applying an etching solution to surfaces of said substrate and said gate wiring and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface of the wiring and the insulating surface by the step of applying the etching solution; and then

forming a gate insulating film and a semiconductor film over said gate wiring, continuously after the contaminating impurities are removed from the surfaces.

28. A method according to claim 27, wherein said etching solution is selected from the group

consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500).

29. A method according to claim 27, wherein the contaminating impurity is at least one element selected from periodic table group 1 elements or periodic table group 2 elements.

30. A method according to claim 27 wherein the contaminating impurity element is at least one element selected from the group consisting of Na, K, Mg, Ca, and Ba.

31. A method according to claim 11, wherein said etching solution is selected from the group consisting of hydrofluoric acid, dilute hydrofluoric acid, ammonium fluoride, buffered hydrofluoric acid (BHF), hydrofluoric acid and aqueous hydrogen peroxide (FPM), and a solution mixture including ammonium hydrofluoride ($NH_4HF_2$) and ammonium fluoride ($NH_4F$) ( LAL500).

32. A method according to claim 15, wherein the contaminating impurity is removed by an acidic solution containing fluorine.

33. A method according to claim 19, wherein the contaminating impurity is removed by an acidic solution containing fluorine.

34. A method according to claim 23, wherein the contaminating impurity is removed by an

acidic solution containing fluorine.

35. A method according to claim 27, wherein the contaminating impurity is removed by an acidic solution containing fluorine.

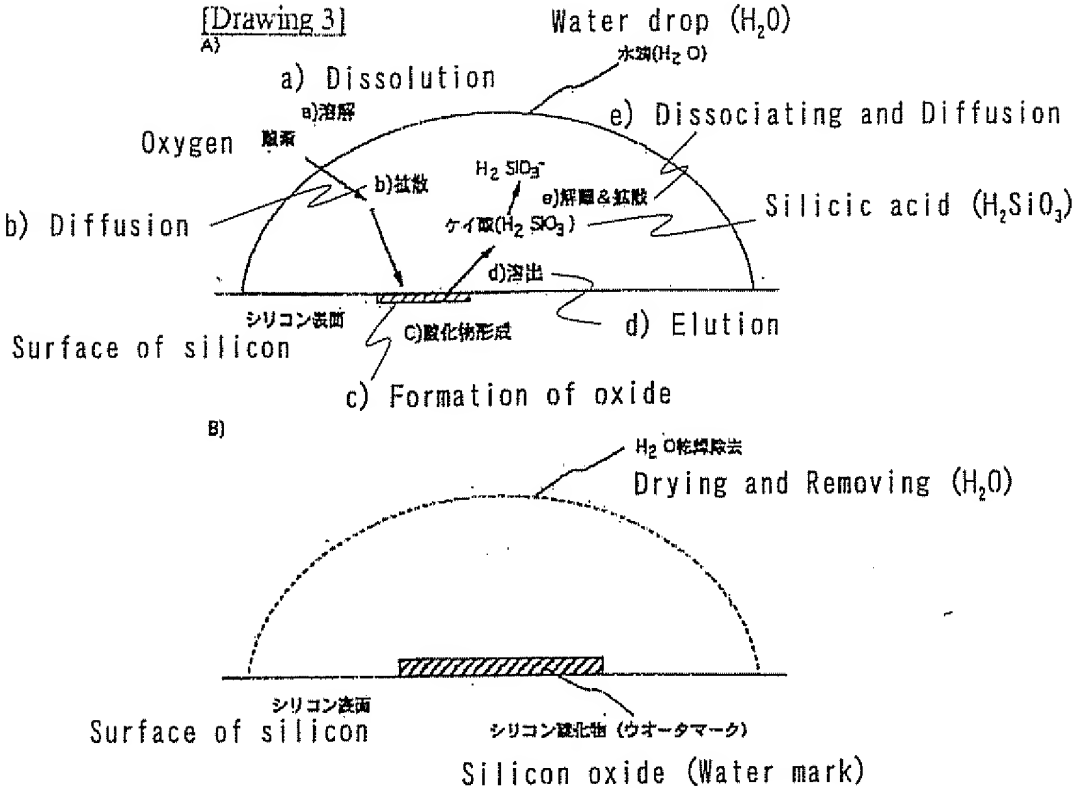
36. A method according to claim 19, wherein the step of crystallization is performed by irradiating the semiconductor film with a laser light.

## ix. EVIDENCE APPENDIX

1. Translation of Drawings 3A and 3B of Chiyou; filed with Response of November 1, 2006 which was entered by the Examiner in the Advisory Action of November 13, 2006.

English Translation of
Drawings 3A and 3B of
Chiyou et al. (JP 11-016866)

[Drawing 3]



## x. RELATED PROCEEDINGS APPENDIX

None